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Update on Parts SEE Susceptibility from Heavy Ions

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13. ABSTRACT (*Maximum 200 words*)

Jet Propulsion Laboratory (JPL) and Th e Aerospace Corporation have collected a fourth set of heavy ion single event effects (SEE) taest data since their last joint contributions to *IEEE Transactions on Nuclear Science* in December 1985, 1987, and 1989. Trends in SEE susceptibility (including soft errors and latchup) for state-of-the-art parts are displayed.

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PREFACE

Special thanks are due to Jim Coss, SEE group leader; Charles Barnes; John Zoutendyk; Peter Wang; Mike Havener; and Mike O'Connor, of JPL.

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INTRODUCTION

An ongoing single event (SEE) test program at JPL and The Aerospace Corporation continues, not only to assess specific part performance for interplanetary and satellite environments, but also to establish trends in SEE response of an ever-increasing body of device data.

In 1985, Nichols et al. [1] published the first nearly comprehensive listing of SEE test data for 186 parts. This presentation was updated in 1987 with the publication [2] of data for 83 additional parts and again in 1989 [3] with data for 154 more parts. In this report, the authors extend the data base for 182 new parts. As before, the data are collected according to technology, function, and manufacturer in order to identify trends, generalizations, and data gaps.

TESTING APPROACHES

The experimental procedures used by JPL and The Aerospace Corporation are evolutionary and are described in detail in previous reports [4,5]. In general, the procedures comply with the guidelines for SEE testing set forth by the ASTM F1.11 document [6].

ORGANIZATION AND SCOPE OF DATA

This report summarizes soft-error and latchup experimental test data from JPL; The Aerospace Corporation; the Applied Physics Laboratory, Johns Hopkins University (JH); Centre National D'Etudes Spatiales (CNES, France); European Space Agency (ESA); and other SEE testers. These data were provided directly to JPL or were otherwise made available to the scientific community during the two-year period from January, 1989, through December, 1990. The authors will include smaller SEE data sets generated by all U.S. and foreign researchers when these data are made directly available. Not included are proprietary data generated by subcontractors who used JPL hardware. Also omitted are now fairly extensive data sets on power MOSFET failures obtained by JPL, Rockwell International, Boeing, and others—such data require a significantly more complicated organization.

The SEE data presented here and in the previous three reports [1–3] represent a substantial majority of all test data obtained on SEE throughout the world. Some of the remaining data may be found in previous issues of *IEEE Transactions on Nuclear Science*, other journals, or in published and unpublished presentations of SEE symposia.

The data from all organizations are summarized and collected together, even though there are minor differences in the data from each organization. For example, JPL defines the threshold linear energy transfer (LET) as that value of LET where soft errors are first counted at fluences of 10^6 ions/cm^2; The Aerospace Corporation currently defines their LET threshold as that point where the measured upset cross section is one percent of the measured maximum cross section. These two values may be quite different.* To obtain accurate single event upset (SEU) rates for a

* The use of an LET threshold defined as a stated percentage of a maximum (saturated) cross section attempts to establish a practical lower bound for the purpose of estimating upset rates. The discrepancy between this definition and JPL's definition becomes academic when a complete cross section is used in rate calculations.

prescribed radiation environment, one requires the entire plot of cross section versus LET, which may be available from the parent test organization.** More recent JPL data may be accessed directly from JPL's computer data base, RADATA.

All data are conveniently divided into two tables: Table 1, for MOS devices, and Table 2, for a shorter list of recently tested bipolar devices. In addition, a new table of data for "Latchup Tests Only" (invariably CMOS processes) are given in Table 3. Those devices having both soft-error and latchup data are reported in Table 1. All data listed here represent a substantial abbreviation and ignore statistical features altogether. SEE tests use a dynamic nominal bias; latchup tests are usually performed at the maximum value of the nominal bias range—a condition that usually (but not always) enhances the possibility of latchup. Unreported transients and higher test temperature measurements may exist for some parts. Therefore, a system designer interested in a specific part is urged to contact the appropriate test organization for further information.

Users are cautioned that manufacturers (listed with their abbreviations in the Appendix) may often change their process (and resultant SEE susceptibility) without changing the part number or notifying tester organizations. Thus, a test of flight parts is always a good policy.

TRENDS

Some trends in the recent data are offered in the "Remarks" column, but for the most part the table speaks for itself. Special studies (such as SEE response variation with temperature, or latchup susceptibility versus epi-layer thickness) are beyond the scope of this presentation.

** More detailed data are available in JPL Publication No. 88-17 by D. K. Nichols et al., "Heavy Ion Induced Single Event Phenomena (SEP) Data for Semiconductor Devices from Engineering Testing" (July, 1988). This report includes cross sections and identification of ions and beam angles.

CONCLUSIONS

The new data presented here can be combined with data given in References [1–3] to develop certain generalizations useful for protecting flight electronics from SEE. Hard technologies and unacceptably soft technologies can be flagged. In some instances, specific tested parts can be taken as candidates for key functions—such as microprocessing or memory. As always with radiation test data, specific test data for qualified flight parts are recommended for critical applications. Calculations of accurate SEE rates will require the assistance of a computer code, a well-defined environment (in terms of flux versus LET), and a complete device characterization (cross section versus LET, at the appropriate temperature). Evaluation of catastrophic effects requires its own statistics in which flares are considered. JPL's recent concerns with power transistor burnout and single-event gate rupture are beyond the scope of this report. The Aerospace Corporation's exploration of SEE transients in linear devices may later open up a whole new concern for a device category formerly considered to be no problem.

TABLE 1 SEU DATA
1989-1990 (MOS AND NMOS DEVICES)

Test Org*	Device	Function	Technology	Mfr.†	Bits	Effective LET** Threshold	Device Cross Section (cm2)***	Cross Section Per Bit (sq mic)	Facility ****	Remarks
CNES	EF6821CM	Peripheral to 6800 microproc.	NMOS	THO	48 tested	5	2E-3	—	88-in & IPN	With Aerospace at 88-in. Feb '89. Same results with IPN Tandem. Device is an interface adapter.
CNES	80C31L	MicroP (8-bit)	CMOS/EPI	MTA	128x8 RAM	~3	2E-3	100	88-in	No latchup at LET = 40 with Aerospace at 88-in. Feb. '89.
SNL	SA3300	MicroP (16-bit)	CMOS/bulk No resistor	SNL	—	35 (2 micron feature size) 23 (1.75/1.25 feature size)			BNL	See F.W. Sexton et al, IEEE NS-37, p1861 (Dec. '90). Compare JPL ('88)
J	SA3304	Peripheral to SA3300	above	SNL	—	40	—	—	BNL & 88-in	Similar to NS32201. 10/88 and 11/89. Current surges. Ambient T = 85C
J/JH	80C86RH	MicroP (16-bit)	CMOS/epi	HAR	—	3	—	—	88-in	JPL: Mask No. 3227, Feb. '89 JH: DC 8817. No latchup at LET = 75.
J	80C86RRH	MicroP (16-bit)	CMOS/epi	HAR	—	3	1/2 of above cross section.	—	88-in	Mask 3582; half of elements are hard. Feb. '89
J	HS82C54RH	Peripheral to 80C86	CMOS	HAR	96	22	—	—	88-in	No latchup at 125 degrees C. Feb'89 Programmable Interval Timer
CNES	MD82C54	Peripheral to 80C86	CMOS/epi (12-micron)	HAR	160	10	4E-4	—	88-in	Latchup at LET = 60. Feb, '89 Thick epi permits latchup!
J	HS82C85RH	Peripheral to 80C86	CMOS	HAR	3 out of 49	22	—	—	88-in	No latchup at T=70 deg. C. Feb. '89. Clock Generator.
CNES	P1750A	MicroP (16-bit)	CMOS/EPI	PFS	—	5±1	Partial	—	IPN	F9450-compatible. Chapuis '90. LU and SEU have same cross section.
A	BX1750A	MicroP (16-bit)	CMOS/epi	ALS	—	20	5E-4	—	88-in	LU LET > 100. May '90.
J	MAS281	MicroP (16-bit)	CMOS/SOS	MED	~200 tested	180	No upset	No Upset	88-in	1750-compatible. Test 504 MeV Xe @ 70 degree angle. May '89

*J = JPL, A = Aerospace Corp., R = Rockwell Int. or IRT (J. Pickel), SNL = Sandia, NTT = Nippon Tel & Tel Corp., IBM = IBM, H = Hughes (El Segundo, CA), LIN = Lincoln Labs, M.I.T., CNES = Centre National d'Etudes Spatiales (France), GD = General Dynamics (J. Elliott at SEE Symposium, April, '90), ESA = European Space Agency JH = John Hopkins Applied Physics Lab.

**LET is Linear Energy Transfer = the density of ionization along an ion's path in MeV/(mg/cm^2).

***Unless otherwise noted, the cross section (upsets/fluence per device) is given for 120-360 MeV krypton (or bromine) at normal incidence, having an LET = 37-40 MeV/(mg/cm^2).

****Cf = Cf-252 isotope facility; BNL = Brookhaven National Laboratory (Long Island, NY) Tandem Van de Graaff; GANIL = Cyclotron (Caen, France); IPN = Tandem Van de Graaff at Institut de Physique Nucleaire (Orsay, France); 88-in. = Cyclotron UC Berkeley, ESA = European Space Agency site.

†See listing in Appendix.

TABLE 1 SEU DATA (CONT'D)
1989-1990 (MOS AND NMOS DEVICES)

Test Org*	Device	Function	Technology	Mfr.†	Bits	Effective LET** Threshold	Device Cross Section (cm2)***	Cross Section Per Bit (sq mic)	Facility ****	Remarks
IBM	80386	MicroP (32-bit)	CMOS/epi CHMOS III	INT	100	6	—	~100	CI-252 & BNL	No latchup. No SEUs from alphas and protons. April '89.
IBM	80386	MicroP (32-bit)	CHMOS IV	INT	100	6	—	~100	Previous	Latchup cross section = 1E-5 cm^2.
Saab Space	80386	MicroP (32-bit)	CHMOS IV	INT	—	—	—	80	CI-252	5-micron epi.
JH	ADSP2100A	Digital Signal Processor	CMOS/epi	ADI	—	13	—	—	BNL	Test of 5 developmental parts with varying epi thickness & n-well dimensions. R.H. Maurer (8/90).
A	ADSP2100A	DSP	—	ADI	—	—	—	—	88-In	LU LET = 12; 1E-3 cm^2. Feb. '90.
LIN	56001	DSP	CMOS	MOT	Memory	~3	—	—	BNL	LU(th)=8. Aug 90. V. Sferrino-LIN
A	CY7C189-15DC	SRAM	CMOS	CYP	16X4	1	2E-4	—	88-In	LU LET = 8; 1E-4 cm^2. May '90.
J/A	CMM6167	SRAM	CMOS/SOS	RCA	16Kx1	15	4E-4	3	88-In	High temp data available. 10/87; 6/88; 2/89.
CNES	MA9167	SRAM	CMOS/SOS	MED	16Kx1	>72	No upset	No upset	IPN	No latchup. 1.5 micron technology. Feb. '90
Saab	IDT7187 Spare	SRAM	NMOS/CMOS	IDT	64Kx1	—	—	—	CI-252	Latchup (S. Mattsson, Saab Space) Compare earlier Aerospace 6/87 and below.
Boeing	IDT7187	SRAM	NMOS/CMOS	IDT	64Kx1	—	—	—	Van deG	LU(th) = 6 LU cross section = 5E-4 cm^2. IEEE (NS '90). See above.
A/JH	IDT71256	SRAM	NMOS/CMOS	IDT	32Kx8	2.5	0.2	—	88-In	A: Latchup at LET = 15, 12/87. JH: Agrees 8/90.
A	S32KX8	SRAM	CMOS	SEI	32Kx8	3	0.1	—	88-In	LU<40 with 1E-3 cm^2. Feb. '89.
A	OW5962	SRAM	CMOS	OWI	32Kx8	8	5E-2	—	88-In	LU = 22 with 3E-3 cm^2. July '89.
A	P4C188L	SRAM	CMOS	PFS	16Kx4	5	2E-2	—	88-In	LU= 11 with 8E-3 cm^2. Sep. '89.
LIN	MT5C1608	SRAM	—	MIC	2Kx8	<1.4	—	—	BNL	LU(th) <26. Aug 90. Sferrino-LIN
CNES	M2568C	SRAM	—	MIC	32Kx8	<1.7	~0.5	—	IPN	No latchup. Feb'90. Compare below.
A/LIN	MT5C2568	SRAM	CMOS/NMOS	MIC	32Kx8	<1.4	~0.6	—	88-in & BNL	LU LET=15 with 1E-5 cm^2. A: 1/89. Multiple soft errors per ion. LIN: 8/90
A	IMS1600SL	SRAM	NMOS	INM	64Kx1	<3	>0.2	—	88-In	LU LET = 15; >2E-3 cm^2. Mar. '90.
CNES	IN1630SL	SRAM	—	INM	—	1.7	0.2	—	IPN	Latchup at LET <<12. Feb. '90.
A	UPD43256	SRAM	NMOS/CMOS	NEC	32Kx8	3	0.4	—	88-In	No latchup. May '90.
A	84256	SRAM	CMOS	FUJ	32Kx8	<3	1	—	88-In	LU LET = 25, 6E-5 cm^2. Nov. '89.
ESA	HM6116	SRAM	NMOS/CMOS?	HIT	2Kx8	5	—	500	IPN	LU LET(th) <13; LU cross section = 3E-4 cm^2. Harboe-Sorensen Dec. '90.
ESA	HM6264	SRAM	—	HIT	8Kx8	~5	—	150	IPN	LU LET(th) < 13; LU cross section = 1E-3 cm^2. Harboe-Sorensen Dec. '90.
LIN	DPS92256	SRAM	—	HIT	32Kx8	<1.4	3E-2	--	BNL	NoLU >54. 8/90. Sferrino-LIN
JH	71256	SRAM	—	HIT	32Kx8	4	0.1	40	BNL	No latchup. 8/90. Compare to IDT71256 listed above.
J/A	HM628128	SRAM	NMOS/CMOS	HIT	128Kx8	4	0.6	60	88-In	Latchup at LET = 80. J: Mar. '90. A: May '90.
LIN	DPS92256	SRAM	—	SNY	32Kx8	~3	—	—	BNL	LU(th)≤26; 6E-6 cm^2, Aug 90.
A	CXK58225	SRAM	CMOS	SNY	32Kx8	9	0.1	–	88-In	LU LET = 25; 4E-4 cm^2. May '90.
A	CXK581000P	SRAM	NMOS/CMOS	SNY	128Kx8	3	0.8	–	88-In	LU LET = 55; 2E-5 cm^2. Feb. '90.
A	MSM8128SLMB	SRAM	CMOS	NEC	128KX8	4	0.6	–	88-In	LU LET = 85 1E-6 cm^2. May '90.

TABLE 1 SEU DATA (CONT'D)
1989-1990 (MOS AND NMOS DEVICES)

Test Org*	Device	Function	Technology	Mfr.†	Bits	Effective LET** Threshold	Device Cross Section (cm2)***	Cross Section Per Bit (sq mic)	Facility ****	Remarks
J	51C98	SRAM	CXMOS/epi	INT	16Kx4	3	6E-2	100	88-in	Latchup at LET = 40. 10/90.
ESA	TC5516	SRAM	CMOS	TOS	2Kx8	~6	—	300	IPN	LU < 27; 1E-4 cm^2. Harboe-Sorensen 12/90.
CNES	TMS—	SRAM	HCM0S3	THO	16K	6	4E-2	—	IPN	LU LET(th) > 54. Chapuis '90.
A	HC6116KSH-T	SRAM	CMOS	HON	2Kx8	25	2E-2	—	88-in	No latchup. Dec. '89.
HON	HC6364	SRAM	CMOs/epi (4-mic epi)	HON	8Kx8	>90	—	—	BNL	Extensive data available at high temps and resistor values, other than 500 ohms used here. Sept. '89.
ESA	HM6504	SRAM	CMOS	HAR	4Kx1	5	—	200	IPN	LU LET(th) = 13; LU cross section = 1E-4 cm^2. Dec '90.
ESA	HM6516	SRAM	CMOS	HAR	2Kx8	4	3E-2	200	IPN	LU LET(th) < 15; LU cross section = 6E-4 cm^2. Dec '90.
J	HM6516	SRAM	CMOS/epi (12 microns)	HAR	2Kx8	<<6	2E-2	120	88-in	Latchup with Kr. Feb. '89. An earlier test with Cf-252 failed to indicate latchup due to low range of Cf-252 ions.
CNES	HM65162	SRAM	CMOS/epi	MTA	2Kx8	—	—	—	IPN	No latchup with 212 MeV Br. Feb. '89. JPL saw latchup at LET << 40. Apr. '87.
CNES	HM65262	SRAM	CMOS/bulk	MTA	16Kx1	—	—	—	GANIL & IPN	Latchup LET < 16. 10/89; 2/90.
CNES	HM65262	SRAM	CMOS/epi	MTA	16Kx1	3	5E-2	300	IPN	No latchup at LET = 72. Feb 90.
CNES	HMS65641	SRAM	CMOS/epi (12 micron)	MTA	8Kx8	2.5	0.2	300	GANIL & IPN	Latchup LET = 50. Date Code: 8930. See Chapius IEEE NS 12/90.
A	2164A	DRAM	NMOS	INT	64K	~1	0.2	300	88-in.	Cross section vs LET given by T. Bion, IEEE Trans. NS-36, p2283 (Dec 89).
ESA	TMS4416	DRAM	NMOS	TIX	16Kx4	<5	—	200	IPN	R. Harboe-Sorensen et al, IEEE Trans Nuc. Sci. NS-37, p1938 (Dec 90).
J	MT1259	DRAM	NMOS	MIC	256K	<1	—	—	BNL	See J. Zoutendyk, IEEE Trans NS-36, p 2267 (Dec. 89) and earlier data.
A	28C256L	EEPROM	CMOS	ATM	32Kx8	10	2E-3	—	88-in	No LU >100. Sep '89.
GD	28C256	EEPROM	—	SEQ	32Kx8	—	3E-6	—	Cf-252	Bradley et al, Latchup. See "Latchup Only" table.
A	28C256-250	EEPROM	CMOS/epi	SEQ	32Kx8	3 to 10	2 to 10E-4	—	88-in	No latchup. May '90.
JH	28C256	EEPROM	CMOS	SEQ	32Kx8	—	—	—	BNL	No soft errors nor LU at LET<120.
LIN	CJ28C256	EEPROM	—	SEQ	32Kx8	—	—	—	BNL	No LU >54. Aug 90. Sferrino-LIN
JH	28C256	EEPROM	CMOS	XIC	32Kx8	—	—	—	BNL	Latchup LET <<37. See LU Table.
A	27HC642	UVEPROM	CMOS	ATM	8Kx8	12	5E-5	—	88-in	No LU >100. Sep '89.
A	CY7C263	UVEPROM	CMOS	CYP	8Kx8	10	—	—	88-in	LU=15 with 2E-3 cm^2. Sept '89.
GD	HM6617	PROM	CMOS/epi	HAR	2Kx8	—	3E-6	N/A	Cf-252	Output buffer upsets.
J	HS-1-6617RH	PROM	CMOS/epi	HAR	2Kx8	19	2E-5	N/A	88-in	Address register upsets in all "0's" mode. No latchup at LET=120. Oct '90.

TABLE 1 SEU DATA (CONT'D)
1989-1990 (MOS AND NMOS DEVICES)

Test Org*	Device	Function	Technology	Mfr.†	Bits	Effective LET** Threshold	Device Cross Section (cm2)***	Cross Section Per Bit (sq mic)	Facility ****	Remarks
A/GD	LL7320Q	Gate Array	CMOS	LSI	64	—	—	—	A: 88-in GD: Cf-252	A: LU LT = 25, 1E-2 cm^2, Jan. '89. GD: Latchup @ 55° C = 1E-4 cm^2, 4/90.
A	LRH9320Q	Gate Array	CMOS/epi	LSI	64	30	3E-4	500	88-in	No LU>100. Jan '89.
A	LRH91000	Gate Array	CMOS/epi	LSI	—	50	—	3	88-in	LU LET >100. Mar '90.
CNES	XC3042	FP Gate Array	CMOS	XIL	285X106	6	3E-2	—	IPN'	LU LET(th)<13. Actel family. Chapuis '90.
CNES	XC2064	FP Gate Array	CMOS	XIL	160x73	6	2E-2	—	IPN	LU LET(th)=12. Actel family. Chapuis '90.
A	ACT1010	FP Gate Array	CMOS/epi	ACT	1200 gates	25	—	500	88-in	No latchup. Feb '90. 10 micron epi.
A	ACT1020	FP Gate Array	CMOS/epi	ACT	2000 gates	25	—	500	88-in	Same as previous.
JH	ACT1020	FP Gate Array	CMOS/epi	ACT	266 F/F	22	—	230	BNL	Compare to above. J.D. Kinnison 1/91.
JH	ACT1020B	FP Gate Array	CMOS/epi	ACT	266 F/F	25	—	230	BNL	"Remarkably similar to above." J.D.K.
A	EP910JC-40	PAL	CMOS	ALT	—	4	—	—	88-in	LU=15 with 7E-4 cm^2. Dec '89.
A	CS5016	A/D Converter	CMOS	CRY	—	10	0.1	—	88-in	LU LET=15; 1E-1 cm^2. May '90.
LIN	PCT245	Transceiver	—	PFS	—	—	—	—	BNL	LU(th) ≤26; 4E-6 cm^2. Aug 90
A	C12014-0001	Op Amp	CMOS	HAR	—	3	1E-3 (spikes)	—	88-in	No latchup. May '90.
A	54AC163	LOGIC	FACT/epi	NSC	—	40	2E-5 (1)	—	88-in	No LU >120. Dec '89. Part D.C. 8909.
A	54AC163	LOGIC	No epi	NSC	—	—	—	—	88-in	Latchup. See LU Only Table. Feb '90.
A	54AC174	LOGIC	FACT/epi	NSC	—	55	3E-5(1)	—	88-in	No LU >120. Dec '89. Part DC 8922.
A	54ACT174	LOGIC	FACT/epi	NSC	—	60	9E-5(1)	—	88-in	No LU >120. Aug '89. Part DC 8920.
A	54AC299	LOGIC	FACT/epi	NSC	—	50	3E-5(1)	—	88-in	No LU>120. Dec '89. Part DC 8922.
A	54AC299	LOGIC	No epi	NSC	—	—	—	—	88-in	Latchup. See LU Only Table. Feb '90.
A	54ACT373	LOGIC	FACT/epi	NSC	—	40	2E-4(1)	—	88-in	No LU>120. Dec '89. Part DC 8948.
A	54FCT374	LOGIC	CMOS	IDT	—	55	4E-6	—	88-in	No LU >100. Feb '89.
A	54HC109	LOGIC	HCMOS	TIX	—	100	3E-6(1)	—	88-in	No latchup. Mar '90.
A	54HC164	LOGIC	HCMOS	TIX	—	40	4E-5(1)	—	88-in	No latchup. Mar '90.
A	54HCT174F	LOGIC	HCMOS/T	RCA	—	20	2E-4	—	88-in	No LU>100. May '89.
A	54HCT373J	LOGIC	HCMOS/T	TIX	—	50	2E-5	—	88-in	No LU>100. May '89.
A	54HC374	LOGIC	HCMOS	TIX	—	60	1E-4(1)	—	88-in	No latchup. Mar '90.

(1) Aerospace cross sections for AC and HC parts are obtained with Xe or high-angle Kr. Aerospace attempts to find the asymptotic limit at high LET. FACT = Fairchild Advanced CMOS Technology. *The NSC FACT process uses 8 micron epi. Those devices with data code 8820 or later are impervious to latchup at LET=120 MeV/(mg/cm²).*

TABLE 2 SEU DATA
1989-1990 (BIPOLAR DEVICES)

Test Org*	Device	Function	Technology	Mfr.†	Bits	Effective LET** Threshold	Device Cross Section (cm2)***	Cross Section Per Bit (sq mic)	Facility ****	Remarks
J	2901C	4-Bit Slice	ECL/TTL	AMD	64	<< 3.3	3E-3	5000	CIT/88in	Feb. '89.
CNES	2910	ROM Sequencer	TTL	AMD	87 tested	3	4E-3	~5000	88-in	Report by Chapuis; with Aerospace (Feb.'89).
A	AM27S49A	PROM	Bipolar	AMD	—	7	9E-5	—	88-in	Dec. '89.
J	93451	PROM (fusible)	STTL Tri-State	FSC	1KX8	> 37	—	—	BNL	Correction to data. Jan '88.
A	54S189	SRAM	STTL	AMD	16x4	3	5E-3	8000	88-in	Feb. '90.
J/A	93L422	SRAM	LTTL	FSC	256x4	1.8	2E-2	2000	88-in	See IEEE NS-36, p 2283 (Dec. '89).
A	54F189	SRAM	F/TTL	NSC	16Kx4	3	2E-3	—	88-in	May '90.
A	54F74	D FF	F/TTL	SGN	2	8	1E-4	5000	88-in	Feb. '89.
A	54F373	Latch	F/TTL	FSC	8	< 15	2E-4	2500	88-in	Nov. '89.
J	54ALS373	Latch	ALS-TTL	TIX	8	4	4-E4	5000	88-in	Feb. '89.
A	54S74	D FF	S/TTL	TIX	2	20	1E-4	5000	88-in	Jan. '89.
GD	AD7543	DAC (12-bit)	—	ADI	—	—	4E-6	—	Cf-252	No latchup. Bradley et al. Dec '90.
J	AD573	A/D (10-bit)	I^2L	ADI	—	13	—	—	88-in	May & Nov. '89.
GD	MP7683	A/D/ (8-bit)	Flash	MPS	—	—	4E-6	—	Cf-252	No latchup. Bradley et al. Dec '90.
J	TDC1048J6A	A/D (8-bit)	Bipolar hybird	TRW	279	~5	—	—	88-in	May & Nov., 1989, Temp=96 deg C. Same SEU response as part below.
J	TDC1048J6C	A/D (8-bit)	Bipolar hybird	TRW	279	~5	—	—	88-in	May & Nov., 1989. Temp=96 deg C. Same SEU response as part above.

*J = JPL,A = Aerospace Corp., R = Rockwell Int. or IRT (J. Pickel), SNL = Sandia, NTT = Nippon Tel & Tel Corp., IBM = IBM, H = Hughes (El Segundo, CA), LIN = Lincoln Labs, M.I.T., CNES = Centre National d'Etudes Spatiales (France), GD = General Dynamics (J. Elliott at SEE Symposium, April, '90), ESA = European Space Agency, JH = John Hopkins Applied Physics Lab.

**LET is Linear Energy Transfer = the density of ionization along an ion's path in MeV/(mg/cm^2).

***Unless otherwise noted, the cross section (upsets/fluence per device) is given for 120-360 MeV krypton (or bromine) at normal incidence, having an LET = 37-40 MeV/(mg/cm^2).

****Cf = Cf-252 isotope facility; BNL = Brookhaven National Laboratory (Long Island, NY) Tandem Van de Graaff; GANIL = Cyclotron (Caen, France); IPN = Tandem Van de Graaff at Institut de Physique Nucleaire (Orsay, France); 88-in. = Cyclotron UC Berkeley, ESA = European Space Agency site.

†See listing in Appendix.

TABLE 3 LATCHUP TEST DATA ONLY
1989-1990

Test Org*	Device	Function	Technology	Mfr.†	Facility****	Results (LET** = MeV/(mg/cm^2))
CNES	ES 10050	ASIC	CMOS/epi	—	IPN	Date Code: 9016. LU(LET) = 25; 1E-4 cm^2. 12-micron epi. Chapuis IEEE NS (12/90).
J	ADSP1016A	Multiplier	CMOS	ADI	88-in	Latchup LET << 37. Cross section (Kr) = 4E-4 cm^2.
GD	IDT7210	Multiplier	CMOS	IDT	Cf-252	Cross section = 1.3E-5 cm^2 @ 85 C; 5E-7 cm^2 @ rm T. SEE Symp 4/90.
GD	DDC61553	1553 Bus Controller	Hybrid	DDC	Cf-252	Latchup
JH	TMC2310	FFT Processor	CMOS	TRW	BNL	No latchup LET >75. Kinnison '91.
A	320C30	DSP	CMOS/epi	TIX	88-in	LU(LET) = 13; 4E-3 cm^2. Nov. '90.
A	320C25	DSP	CMOS	TIX	88-in	LU(LET) = 12; 1E-3cm^2. Sep '89.
JH	320C25	DSP	CMOS/epi	TIX	BNL	One with LU LET< 26; other with LU LET = 53. Aug. '90.
CNES	320C25	DSP	CMOS/epi	TIX	GANIL	Latchup LET << 37; < 1E-2 cm^2. Date Code 8917, Oct. 1989.
CNES	320C25	DSP	CMOS/epi	TIX	IPN	Feb '90. This data from Tandem did not properly locate latchup threshold with oblique angles because of limited beam range. DKN.
CNES	ZR34161	Signal Processor	CMOS/epi (12-micron)	ZOR	GANIL & IPN	Latchup LET 17 ± 5; 4E-3 cm^2. Oct. '89 and Feb. '90.
JH	ADSP2100 & 2100A	DSP	CMOS	ADI	BNL	LU = 14 for each device type.
A	ADSP2100ASG	DSP	CMOS	ADI	88-in	LU LET = 12; 1E-3 cm^2. Feb. '90.
JH	56001	DSP	CMOS	MOT	BNL	Latchup LET < 26. Aug. '90.
CNES	MC68882	Flt. Pt. Unit (32-bit)	CMOS/epi (15-micron)	MOT	IPN	Latchup LET threshold = 12. LU cross section = 2E-3 cm^2. See Chapuis IEEE NS (12/90).
CNES	MHS80C31	MicroCont. (8-bit)	CMOS/epi (8-micron)	MTA	GANIL	Latchup > 37; 4E-6 cm^2. Date Code 8921, October '89.
CNES	MHS80C31	MicroCont. (8-bit)	CMOS/epi (10-micron)	MTA	IPN	Latchup < 25; 2E-6 cm^2. Feb. '90.
JH	RX2000	MicroP	CMOS/epi	HAR	BNL	LET>120. Kinnison '91.

*J = JPL, A = Aerospace Corp., R = Rockwell Int. or IRT (J. Pickel), SNL = Sandia, NTT = Nippon Tel & Tel Corp., IBM = IBM, H = Hughes (El Segundo, CA), CNES = Centre National d'Etudes Spatiales (France), GD = General Dynamics (J. Elliott at SEE Symposium, April, '90), ESA = European Space Agency, JH = John Hopkins Applied Physics Lab.
**LET is Linear Energy Transfer = the density of ionization along an ion's path in MeV/(mg/cm^2).
****Cf = Cf-252 isotope facility; BNL = Brookhaven National Laboratory (Long Island, NY) Tandem Van de Graaff; GANIL = Cyclotron (Caen, France); IPN = Tandem Van de Graaff at Institut de Physique Nucleaire (Orsay, France); 88-in. = Cyclotron UC Berkeley, ESA = European Space Agency site.
Note: Unless otherwise noted, the cross section (upsets/fluence per device) is given for 120-360 MeV krypton (or bromine) at normal incidence, having an LET = 37-40 MeV/(mg/cm^2).
†See listing in Appendix.

TABLE 3 LATCHUP TEST DATA ONLY (CONTINUED)
1989-1990

Test Org*	Device	Function	Technology	Mfr.†	Facility****	Results (LET** = MeV/(mg/cm^2))
CNES	P1750A	MicroP (16-bit)	CMOS/epi (9-micron)	PFS	GANIL & IPN	Latchup <11; 7E-3 cm^2. Oct. '89 & Feb. '90. DC 8918 is 1.25 micron technology.
CNES	P1750AE	MicroP (16-bit)	CMOS/epi (9-micron)	PFS	IPN	Feb. '90. Latchup same as above. One-micron technology. Date Code: 8936.
JH	P1750AE	MicroP (16-bit)	CMOS/epi (9-micron)	PFS	BNL	Static test gives Latchup threshold = 50. See below. Source: J. D. Kinnison '89.
GD	P1750AE	MicroP (16-bit)	CMOS/epi (9-micron)	PFS	—	Dynamic test gives LU = 7. See above. E.C. Smith, Apr. '90.
JH	64500/1	MicroP (16-bit)	CMOS/epi	LSI	BNL	1750A CPU. LU threshold = 75.
JH	68020	MicroP	CMOS	MOT	Cf-252	LU thres < 40. Kinnison '89. Compare with next 4 lines.
CNES	68020	MicroP	CMOS	MOT	IPN	LU thres = 6. Chapuis '90.
JH	68020	MicroP	CMOS/epi	MOT	Cf-252 & BNL	LU thres < 40. 15-micron epi. See above & below.
CNES	68020	MicroP	CMOS/epi	MOT	IPN	LU thres >72. 15-micron epi. Compare above and below. Chapuis '90.
JH	68020	MicroP	CMOS/epi	MOT	BNL	LU thres >50. 12-micron epi. See above 2 lines.
A	7201LA	FIFO	CMOS (512x9)	IDT	88-in	LU =13. Cross section = 2E-3. cm^2. Sep. '89.
JH	7202RT	FIFO	CMOS (2Kx9)	IDT	BNL	Latchup LET < 37. Jan. '91.
JH/NRL	AMD7202	FIFO	CMOS (2Kx9)	AMD	BNL	Latchup LET < 26. Jan. '91.
JH	AMD7204	FIFO	CMOS (4Kx9)	AMD	BNL	Latchup LET < 26. Aug. '90.
A	MP7682	6-bit ADC	CMOS	MPS	88-in	No LU LET >100. July '89.
JH	AD7672	12-bit ADC	CMOS	ADI	BNL	No latchup LET > 75. Kinnison '91.
JH	CS5016	16-bit ADC	CMOS	CRY	BNL	Latchup LET << 37.
JH	7134RT	4Kx8 SRAM	CMOS	IDT	BNL	Latchup << 37. Kinnison '91.
GD	CY7C185	8Kx8 SRAM	CMOS	CYP	Cf-252	Latchup cross section = 2E-4 cm^2 @ 85° C.; 8E-5 cm^2 at rm Temp. SEE Symp Apr. '90.
JH	P4C163	8Kx9 SRAM	CMOS	PFS	BNL	Latchup LET = 30. Jan. '91.
A	P4C164L	8Kx8 SRAM	CMOS	PFS	88-in	LU = 8. Cross section =1E-2 cm^2. Sep. '89.
CNES	MHS65162	2Kx8 SRAM	CMOS/epi	MTA	IPN	No latchup @ LET =72 for 3E5 ions/cm^2. Feb. '90. See CMOS table.
CNES	HM65262	16Kx1 SRAM	CMOS	MTA	GANIL	Latchup LET << 37. Cross Sect > 4E-3 cm^2. Oct. '89.
CNES	61CD16	16K SRAM	CMOS/epi	TIX	IPN	LU LET(th) <13; cross section at LET=40 is 6E-3 cm^2. Chapuis '90. Compare to below.
CNES	61CD64S	64Kx1 SRAM	CMOS/epi	TIX	GANIL	No latchup up to LET = 116.
CNES	MB81C81	256Kx1 SRAM	CMOS tristate	FUJ	IPN	Feb. '90. No latchup at LET = 114 for 1E4 iodine ions/cm^2.
JH	MT5C2568	32Kx8 SRAM	CMOS/epi	MIC	BNL	LU thresh < 40. J Kinnison '89.
J/A	TMS27C256	32Kx8 UV-Erasable PROM	HVCMOS epi/guard rings	TIX	88-in	J: No latchup to LET = 120 up to T = 60 deg C. Nov. '89. A: No latchup. Feb. '90.
GD/JH	28C256	EEPROM (32Kx8)	CMOS	XIC	Cf-252 BNL	GD: Latchup. JH: Latchup << 37.
JH	28C256	EEPROM (32Kx8)	CMOS/epi	SEQ	BNL	LU thresh > 120. See above.
A	28HC64L	EEPROM (8Kx8)	CMOS	ATM	88-in	No LU > 100. Dec. '89.

TABLE 3 LATCHUP TEST DATA ONLY (CONTINUED) 1989-1990

Test Org*	Device	Function	Technology	Mfr.†	Facility****	Results (LET** = MeV/(mg/cm^2))
CNES	SOR 5053	Coder	CMOS	SOR	IPN	LU = 9 ± 3. Chapuis '90.
A	MC10H115FN	Recvr	ECL	MOT	88-in	No LU > 100. Feb. '90.
JH	TSC430	FET Driver	CMOS/epi	TEL	BNL	No LU > 120. JDK '91.
JH	54AC02	Logic	FACT	NSC	BNL	LU thresh > 75. Kinnison '89.
JH	54AC08	Logic	FACT	NSC	BNL	LU thresh > 75. Kinnison '89.
CNES	54AC74	Logic	AdvCMOS/epi	NSC	IPN	No LU > 72. Feb. '90.
A	54AC163	Logic	ACMOS	NSC	88-in	LU LET = 40; 1E-5 cm^2 at high LET. Feb. '90. Date Code 8718. Compare with GANIL data below.
CNES	54AC163	Logic	ACMOS	NSC	GANIL	Latchup LET < 40; > 2E-6 cm^2. Date Code 8718; Oct. '89. Compare above; 2 lines below.
CNES	54AC163	Logic	ACMOS	RCA	GANIL	Latchup LET << 37; >5E-6 cm^2. Date Code 8804; Oct. '89.
JH	54ACT163	Logic	FACT	NSC	BNL	LU thresh > 75. Kinnison '89. Re 2 lines above: J.K. says later DC used here is known LU-proof.
JH	54AC174	Logic	FACT	NSC	BNL	LU thresh > 75. J. Kinnison '89.
JH	54ACTQ174	Logic	FACT w. I/O	NSC	BNL	LU thresh > 120. J. Kinnison expects other ACTQ's are LU proof.
A	54AC245	Logic	ACMOS/epi	NSC	88-in	LU thresh > 120. Dec '88 & Dec. '89.
A	54AC245	Logic	No epi	NSC	88-in	LU LET = 60; 1E-6 cm^2. Feb. '90.
A	54ACT253	Logic	ACMOS/epi	NSC	88-in	No latchup. May '90.
A	54AC299	Logic	No epi	NSC	88-in	LU LET = 60; 2E-5 cm^2. Feb. '90.
A	54ACT374	Logic	No epi	NSC	88-in	LU LET = 50; 5E-6 cm^2. Feb. '90.
JH	P54PCT245	Logic	CMOS	PFS	BNL	LU LET < 40. Kinnison '89.
A	74HC00D	Logic	HCMOS	RCA	88-in	No LU > 100. Feb. '90.
A	54HC03J	Logic	HCMOS	TIX	88-in	No LU > 100. Sept. '89.
A	74HC04D	Logic	HCMOS	RCA	88-in	No LU > 100. Feb. '90.
A	54HC11J	Logic	HCMOS	TIX	88-in	No LU > 100. Sept. '89.
A	54HC32	Logic	HCMOS	TIX	88-in	No LU. Mar. '90.
A	74HC75D	Logic	HCMOS	RCA	88-in	No LU > 100. Feb. '90.
J	54HC139	Logic	HCMOS	TIX	88-in	No LU > 180. May '89.
J	54HC154	Logic	HCMOS	TIX	88-in	No LU > 180. May '89.
A	54HC390J	Logic	HCMOS	TIX	88-in	No LU > 100. Sept. '89.
A	54HC595J	Logic	HCMOS	TIX	88-in	No LU > 100. Sept. '89.
A	54HCT4059	Logic	HCMOS	RCA	BNL	No LU > 75. Kinnison Jan. '91.

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APPENDIX

MANUFACTURER ABBREVIATIONS

ACT	Actel
ADI	Analog Devices, Incorporated
ALS	Allied Signal
ALT	Alpha Industries, Semiconductor Division
AMD	Advanced Microdevices Corporation
ATM	Atmel
CRY	Crystal Semiconductor, Incorporated
CYP	Cypress Corporation
DDC	DDC ILC Data Device Corporation
FSC	Fairchild Semiconductor Corporation
FUJ	Fujitsu ,Ltd.
HAR	Harris Corporation, Harris Semiconductor Division
HIT	Hitachi Ltd.
HON	Honeywell, Incorporated
IDT	Integrated Device Technologies, Incorporated
INM	INMOS Corporation
INT	Intel Corporation
LSI	LSI Logic Corporation
MED	Marconi Electronic Devices
MIC	Micron Technologies
MIT	Mitsubishi
MOT	Motorola Semiconductor Products, Incorporated
MPS	Micro Power System
MTA	Matra Harris Semiconductor
NEC	Nippon Electric Corporation
NSC	National Semiconductor Corporation
OWI	Omni-Wave, Incorporated
PFS	Performance Semiconductor Corporation
RCA	Radio Corporation of America
SEI	Seiko
SEQ	SEEQ Technology, Incorporated
SGN	Signetics Corporation
SNL	Sandia National Laboratories
SNY	Sony Corporation
SOR	SOREP
TEL	Teledyne Crystalonics
THO	Thomson Military & Space, France
TIX	Texas Instruments, Incorporated
TOS	Toshiba
TRW	TRW, Incorporated
XIC	Xicor, Incorporated
XIL	Xilinx Corporation
ZOR	Zoran

TECHNOLOGY OPERATIONS

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